Neural Networks 45 (2013) 1–3

Contents lists available at SciVerse ScienceDirect

Neural Networks

journal homepage: www.elsevier.com/locate/neunet

Editorial

Neuromorphic Engineering: From Neural Systems to Brain-Like Engineered Systems

The styles of computation used by biological systems are fundamentally different from those used by conventional computers: biological neural networks process information using energy-efficient, highly parallel, event-driven architectures as opposed to clocked serial processing. They are composed of multiple instances of heterogeneous elements and are able to self-repair, adapt and learn from the interaction with the environment. Memory in biological systems is distributed throughout the architecture, relying on local bio-chemical machinery for efficient storage and recall. These remarkable biological traits yield a potentially attractive alternative to conventional computing strategies. A special focus of this issue is Neuromorphic VLSI systems that are composed of Very Large Scale Integrated (VLSI) devices with hybrid analog/digital circuits that implement hardware models of biological systems. When implemented in VLSI (including FPGA) technology, neuromorphic systems often exploit strategies similar to those observed in biological systems for maximizing compactness, optimizing robustness to noise, minimizing power consumption, and increasing fault tolerance (Mead, 1990).

By emulating the neural style of computation, neuromorphic architectures can exploit to the fullest potential the features of advanced scaled VLSI processes and future emerging technologies, naturally coping with the problems that characterize them, such as time dependent device variability, and mismatch.

In this Special Issue we expressly called for a broad range of topics related to the common theme of *Neuromorphic Engineering*. The various contributions received actually describe recent developments and progress in understanding the interplay between biology and technology for the developments of bio-inspired systems that reproduce functionality and rapid processing of their biological counterpart. In particular, one of the goals of this Special Issue was to explore the possible synergies and interactions of different perspectives for low-level computation up to the system-level brain-like processing.

This special issue includes 13 papers. They represent about one-half of the submitted manuscripts which underwent a peer reviewed process. They can be roughly subdivided in three broad areas, namely: neuromorphic implementation of Spiking Neural Networks; application of bio-inspired hardware to different problems that involve learning; and architectures in emerging technologies such as memristors. We now give a brief summary for each of the papers in this special issue.

"**Design of Silicon Brains in the nano-CMOS Era: Spiking Neurons, Learning Synapses and Neural Architecture Optimization**", by A.S. Cassidy, J. Georgiou and A.G. Andreou, provides an overview setting for this Special Issue. The paper begins with a historical perspective on neuromorphic engineering (Mead, 1990), followed by a fresh view of Marr's three levels of description, in the context of recent advances in computational sciences. The authors argue that parallel processing under physical constraints provides the theoretical foundation for understanding both neural computation as well as engineering synthetic systems in emerging nano-CMOS technologies. The paper also presents a quantitative architecture design framework. This framework is validated through design exploration of spiking neurons and Spike Time Dependent Plasticity (STDP) learning algorithms in FPGAs. In this architecture neurons are abstracted as digital arithmetic logic units and communications processor. The conclusions of the paper include a summary of ideas and directions for the design of future neuromorphic systems.

João Carneiro, Sio-Hoi Ieng, Christoph Posch, and Ryad Benosman, in the paper "**Event-Based 3D Reconstructions from Neuromorphic Retinas**", present an innovative N-ocular 3D reconstruction algorithm for event-based artificial retina sensors. Event-based artificial retinas capture visual information asynchronously and encode it into streams of asynchronous spike-like pulse data where visual features are implicitly encoded in the spike timings. With the high temporal resolution of the asynchronous visual information acquisition silicon retinas, the output of these sensors is ideally suited for dynamic 3D reconstruction. The technique presented by the authors takes full benefit of the event-driven representation where events are processed just-in-time. This strategy allows to preserve the original dynamics of the scene, hence allowing for more robust 3D reconstructions. As opposed to existing techniques, this algorithm is based on geometric and time constraints alone, making it particularly simple to implement in a scalable fashion.

In "**Computing with networks of spiking neurons on a biophysically motivated floating-gate based neuromorphic integrated circuit**", by Stephen Brink, Stephen Nease, and Paul Hasler, the authors investigate the performance of several spiking neural networks networks simulated on an analog VLSI neuromorphic integrated circuit. The networks are discussed in terms of their computational significance, which includes applications such as arbitrary spatio-temporal pattern generation and recognition, "winner-takes-all" competition, stable generation of rhythmic outputs, and volatile memories. Analogies to the behaviour of real biological neural systems are also noted. The alternatives for implementing the same computations are discussed and compared in terms of computational efficiency. The authors conclude that network simulations on neuromorphic hardware are significantly more power efficient than numerical integration of model equations.

J.M. Barron-Zambrano, and C. Torres-Huitzil in the paper "**FPGA implementation of a configurable neuromorphic CPG-based locomotion controller**" investigate on recent developments of

0893-6080/$ – see front matter
http://dx.doi.org/10.1016/j.neunet.2013.07.001

neuromorphic hardware systems implemented using a hybrid approach that incorporate digital hardware trading off flexibility and scalability at the cost of power efficiency and biological realism. They propose an FPGA-based bio-inspired embedded system on a chip to generate locomotion patterns of periodic rhythmic movements inspired by Central Pattern Generators (CPGs). The proposed implementation follows a top-down approach where modularity and hierarchy are two desirable features. The locomotion control is based on CPG models to produce rhythmic locomotion patterns or gaits for legged robots such as quadruped and hexapods. The architecture is configurable and scalable for robots with either different morphologies or different degrees of freedom. Experiments performed on a real robot are presented and discussed. The authors claim is that the obtained results demonstrate the CPG-based controller provides flexibility to generate different rhythmic patterns at runtime suitable for adaptable locomotion.

In the paper titled "**Nonlinear Spectro-Temporal Features based on Cochlear Model for Automatic Speech Recognition in Noisy Situation**" by Yong-Sun Choi, and Soo-Young Lee, the authors discuss a nonlinear speech feature extraction algorithm that is developed by modeling human cochlear functions. The proposed approach generates a noise-robust front-end valuable for speech recognition systems. The algorithm was based on a model of the organ of Corti in the human cochlea that incorporates basilar membrane (BM), outer hair cells (OHCs), and inner hair cells (IHCs) functionality. Frequency-dependent nonlinear compression and amplification of OHCs were modeled by lateral inhibition to enhance spectral contrasts. The compression coefficients show frequency-dependency based on the psychoacoustic evidence. Spectral subtraction and temporal adaptation is applied in the time-frame domain. With long-term and short-term adaptation characteristics, these factors remove stationary or slowly-varying components and amplify the temporal changes such as on-set or off-set. The performance of the proposed systems are evaluated on a noisy speech database and it is shown that this simulated cochlea outperforms the baseline methods such as Mel-frequency cepstral coefficients (MFCCs) and RASTA-PLP in unknown noisy conditions.

Mostafa Rahimi Azghadi, Said Al-Sarawi, Derek Abbott, and Nicolangelo Iannella, in the paper "**A Neuromorphic VLSI Design for Spike Timing and Rate Based Synaptic Plasticity**", consider Triplet-based Spike Timing Dependent Plasticity (TSTDP) as a powerful synaptic plasticity rule that acts beyond conventional pair-based STDP (PSTDP). Here, the TSTDP it is shown to be capable of reproducing the results from a variety of biological experiments, while the PSTDP rule fails to reproduce them. Additionally, it is shown that the behavior inherent to the spike rate-based Bienenstock–Cooper–Munro (BCM) synaptic plasticity rule can also emerge from the TSTDP rule. This paper proposes an implementation of the TSTDP rule in an analog VLSI circuit designed using the AMS 0.35 μm CMOS process. Simulation results demonstrate how well the proposed circuit can alter synaptic weights according to the timing difference amongst a set of different patterns of spikes. Furthermore, the circuit is shown to give rise to a BCM-like learning rule, which is a rate-based rule. To mimic implementation environment, a Monte Carlo analysis has been conducted on the proposed circuit. The authors claim that this Monte Carlo simulation and the achieved results from fine-tuned circuits show the possibility of mitigating the effect of process variations in the proof of concept circuit, although a practical variation aware design technique is required to obtain a high circuit performance in a large-scale neural network.

Louis-Charles Caron, Michiel D'Haene, Frédéric Mailhot, Benjamin Schrauwen, and Jean Rouat, in the paper "**Event management for large scale event-driven digital hardware spiking neural networks**" analyze Spiking Neural Networks (SNNs), event-driven simulation and digital hardware neuromorphic systems. They note that, despite the popularity of event-driven SNNs in software, very few digital hardware architectures are found. They interpret this as a failure of existing hardware solutions for event management to scale well with the number of events. The paper introduces the structured *heap queue*, a pipelined digital hardware data structure, and demonstrates its suitability for event management. The structured *heap queue* scales gracefully with the number of events, allowing the efficient implementation of large scale digital hardware event-driven SNNs. The scaling is linear for memory, logarithmic for logic resources and constant for processing time. The structured *heap queue* is tested on field-programmable gate array (FPGA) for an image segmentation experiment that implies the use of a SNN of 65 536 neurons and 513 184 synapses. Events can be processed at the rate of 1 every 7 clock cycles and the processed image is segmented in 200 ms.

In the paper "**Learning the Pseudoinverse Solution to Network Weights**" by J. Tapson and A. van Schaik, the authors noted that the computation of the pseudo-inverse by singular value decomposition in the neural network framework is problematic both for biological plausibility and as an online and adaptive method. They thus present an online or incremental method of computing the pseudo-inverse which is biologically plausible as a learning method, and which can be made adaptable for non-stationary data streams. The method is significantly more memory-efficient than the conventional computation of pseudo-inverses by singular value decomposition.

In the second group of papers, we have contributions of bio-inspired architectures in emerging technologies such as memristors. Recently, the research group of Williams built a nanoscale TiO_2 device which exhibits properties of non-volatility and synaptic characteristics (Strukov, Snider, Stewart, & Williams, 2008). The existence of the memristor was first conjectured by L. Chua in 1971 as a flux-controlled two-terminal element that behaves like a nonlinear resistor whose resistance is a function of the charge flowed through the device (Chua, 1971). Memristors show two stable high- and low-resistance states, a feature that allows them to act as non-volatile memory (Chua, 2012). Memristors have high potential for implementing learning synapses since their conductance can be modulated by external stimuli. Memristors are the subject of intensive researches aimed to implement hardware nano-synapses that can achieve Spike-Timing Dependent Plasticity (STDP), and eventually implement VLSI/CMOS neural networks (Ebong & Mazumder, 2012).

In this group of papers, the contribution "**Hierarchical Random Cellular Neural Networks for System-Level Brain-Like Signal Processing**", by Robert Kozma, and Marko Puljic, argues that sensory information processing and cognition in brains can be abstracted using dynamic systems theory. The brain's dynamic state is described by a trajectory evolving in a high-dimensional state space and exploit a hierarchy of random cellular automata as the mathematical tools to describe the spatio-temporal dynamics of the cortex. The corresponding brain model is called neuropercolation which has distinct advantages compared to traditional models using differential equations, especially in describing spatio-temporal discontinuities in the form of phase transitions. Phase transitions demarcate singularities in brain operations at critical conditions, which are viewed as hallmarks of higher cognition and awareness experience. The introduced Monte-Carlo simulations on parallel computing platforms highlight the importance of neuromorphic VLSI implementations, and the high potential of future memristive technologies.

In the contribution "**Adaptive Neuromorphic Architecture (ANA)**", by Frank Zhigang Wang, Leon O. Chua, et al., a novel kind of neuromorphic hardware is proposed which is capable to self-adjust its inherent parameters (for instance, the resonance frequency) following naturally the stimuli frequency. Such an architecture is potentially interesting for brain-like engineered

systems since some parameters of the stimuli are not known in advance. The physical substrate of adaptivity is obtained by introducing circuit elements with memory, namely meminductors or mem-capacitors. They are two-terminal dynamic circuit elements whose properties depend on the current state and the previous history. These devices basically extend the concept of memristors and are considered common at the nano-scale where the dynamical features of electrons and ions depend on the previous events. As a hardware model of biological systems, ANA can be used to adaptively reproduce the observed biological phenomena in amoebae (Pershin, La Fontaine, & Di Ventra, 2008).

A novel analog CMOS design of a cortical cell, that computes weighted sum of inputs, is proposed in the paper "**An adaptive neuromorphic model of ocular dominance map formation using floating gate synapse**" by C.M. Markan, Priti Gupta, and Mukti Bansal Bansal. Here, the cell's feedback regime exploits the adaptation dynamics of floating gate pFET "synapses" to perform competitive learning amongst input weights as time-staggered winner-takes-all. A learning rate parameter regulates adaptation time and a bias enforces resource limitation by restricting number of input branches and winners in a competition. When learning ends, the cell's response favors one input pattern over others to exhibit feature selectivity. Embedded in a 2D RC grid, these feature selective cells are capable of performing a symmetry breaking pattern formation, observed in some reaction-diffusion models of cortical feature map formation, e.g., Ocular Dominance.

It is well known that sparse approximation and signal compression can be mapped as optimization problems in signal and image processing (Morabito, Cacciola, & Occhiuto, 2011). In the paper, "**Configurable Hardware Integrate and Fire Neurons for Sparse Approximation**", Samuel Shapero, Christopher J. Rozell, and Paul Hasler present a Hopfield-Network-like system of integrate and fire (IF) neurons that use the Locally Competitive Algorithm (LCA) to solve an overcomplete L_1 sparse approximation problem. A scalable system architecture is described, including IF neurons with a nonlinear firing function, and current-based synapses to provide linear computation. A network of 18 neurons with 12 inputs is implemented on the RASP2.9v chip, a Field Programmable Analog Array (FPAA) with directly programmable floating gate elements. The system uses over 1400 floating gates, according to the authors' claim, the largest system programmed on a FPAA to date. The circuit successfully reproduced the outputs of a digital optimization program, converging to within 4.8% RMS, and an objective cost only 1.7% higher on average. The active circuit consumed 559 μA of current at 2.4 V, and converges on solutions in 25 μs, with measurement of the converged spike rate taking an additional 1 ms. Extrapolating the scaling trends to a $N = 1000$ node system, the Analog LCA compares favorably with state-of-the-art digital solutions, and analog solutions using a non-spiking approach.

In the paper titled "**Single-hidden-Layer Feed-forward Quantum Neural Network based on Grover learning**", Cheng-Yi Liu, Chein Chen, Ching-Ter Chang, and Lun-Min Shih propose a novel single-hidden-layer feed-forward quantum neural network model which is based on concepts and principles derived from the quantum theory. By combining the quantum mechanism with the feed-forward neural network, quantum hidden neurons and connected quantum weights are defined, and used as the fundamental information processing unit in a single-hidden layer feed-forward neural network. The quantum neurons incorporate a wide range of nonlinear functions that are used as the activation functions in the hidden layer of the network. Through the Grover searching algorithm the optimal parameter setting are derived iteratively, thus making very efficient neural network learning possible. The simulation results reported in the paper show that the resulting neural network that mixes quantum neurons and weights with the Grover searching algorithm based learning, is efficient also in the training phase and could be of interest for many applications.

Overall, the articles proposed in this special issue provide a tapestry of diverse ideas and concepts in the field of neuromorphic systems engineering. They demonstrate the vitality of this interdisciplinary research field as well as its capability to gather a worldwide interest. In particular, it appears that neuromorphic hardware may help to further investigate on a fascinating ability of our brain, namely, creativity. We hope and believe that the readers will find inspiration from these papers to ignite new ideas and research in the years to come.

References

Mead, C. A. (1990). Neuromorphic electronic systems. *Proceedings of the IEEE*, *78*(10), 1629–1636.
Strukov, D. B., Snider, G. S., Stewart, D. R., & Williams, R. S. (2008). The missing memristor found. *Nature*, *453*, 80–83.
Chua, L. O. (1971). Memristor - The missing circuit element. *IEEE Trans. Circuit Theory*, *18*, 507–519.
Chua, L. O. (2012). The fourth element. *Proceedings of the IEEE*, *100*(6), 1920–1927.
Ebong, I. E., & Mazumder, P. (2012). CMOS and memristor-based neural network design for position detection. *Proceedings of the IEEE*, *100*(6), 2050–2060.
Pershin, Y. V., La Fontaine, S., & Di Ventra, M. (2008). Memristive model of amoeba learning. arXiv:0810.4179.
Morabito, F. C., Cacciola, M., & Occhiuto, G. (2011). Creative brain and abstract art: a quantitative study on Kandinskij paintings, Proc. of the Intl. J. Conf. on Neur. Netw., 2387–2394, San Jose, CA, USA. http://dx.doi.org/10.1109/IJCNN.2011.6033528.

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