Resource Efficiency of Scalable Processor Architectures for SDR-based Applications

Thorsten Jungeblut¹, Johannes Ax², Gregor Sievers², Boris Hübener², Mario Porrmann², Ulrich Rückert¹

¹ Cognitive Interaction Technology – Center of Excellence (CITEC), Bielefeld University
² Heinz Nixdorf Institute, University of Paderborn
Motivation: Resource efficient processor architectures

- Increasing complexity of mobile applications
- More functionality
  - New communications standards (LTE Advanced: 1 GBit/s)
  - Multimedia applications (Video, 3-D, ...)
- Static hardware solutions ➔ Flexible software implementations (e.g., Software-defined radio - SDR)

➔ Powerful CPU necessary

- High requirements to resource efficiency!
Motivation: VLIW architectures

- RISC architectures allow for higher performance by increasing clock frequency
  ➔ Power consumption increases
- Parallel architectures enable **high performance** at a **reasonable low clock frequency**
  ➔ High resource efficiency

- Compared to superscalar architectures
  - **VLIW (Very-Long Instruction Word)**-architectures leave the scheduling to the compiler ➔ Low resource requirements
Goal: Automated design flow!
Modular VLIW-architecture
DSE (core level)

- Trade-off between
  - clock cycles
  - clock frequency
  - area requirements
  - power consumption
DSE (core level)

- Trade-off between
  - clock cycles
  - clock frequency
  - area requirements
  - power consumption

The CoreVA architecture

4x ALUs
2x Multiply-accumulate
2x Division-step
2x Load/Store
31 General purpose registers
8 condition registers
CoreVA VLIW-architecture: Key features

- Harvard architecture (LD/ST architecture)
- Six-staged pipeline (non-interlocked)
- Instruction compression
- 31 general purpose registers, 2x8 bit condition register
- 1-cycle-instructions, 1 cycle latency (MLA, BR, LDW: 2 cycles, DIV: 32 cycles)
- Parameterizable instruction alignment buffer (L0-cache)
- ARM-like instruction set (binary compiler)
- Comprehensive pipeline bypass
- 16-bit SIMD mode

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<table>
<thead>
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<tr>
<td>31</td>
<td>27</td>
<td>17</td>
<td>12</td>
<td>7</td>
<td>0</td>
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</tbody>
</table>

41 Base instructions
15 SIMD instructions

32-Bit RISC instructions
DSE (system level): Hardware accelerators (HWACC)

- Data memory
- Hardware extension
- Module number
- Module address

Address decoder

Instruction Fetch
Instruction Decode
Register Read

Instruction memory
Memory

ALU
ALU
ALU
ALU

LD/ST
LD/ST

Condition register

Register

Data memory

HWACC #1
HWACC #2
HWACC #3
### Hardware accelerators (HWACC)

<table>
<thead>
<tr>
<th>Hardware accelerator</th>
<th>Processing Time (Speedup)</th>
<th>Area Requirements</th>
<th>Power consumption</th>
<th>Energy efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC</td>
<td>- 87 % (Speedup: x 8)</td>
<td>+ 0.7 %</td>
<td>+ 0.6 %</td>
<td>x 6.8</td>
</tr>
<tr>
<td>ECC</td>
<td>- 93 % (Speedup: x 14)</td>
<td>+ 30 %</td>
<td>+ 30 %</td>
<td>x 11.0</td>
</tr>
<tr>
<td>IEEE 802.11b</td>
<td>- 88 % (Speedup: x 8)</td>
<td>+ 40 %</td>
<td>+ 19 %</td>
<td>x 6.0</td>
</tr>
<tr>
<td>AES-256</td>
<td>- 99 % (Speedup: x 66)</td>
<td>+ 39 %</td>
<td>+ 54 %</td>
<td>x 43.0</td>
</tr>
</tbody>
</table>

Additional hardware extensions:
- UART (debugging)
- Ethernet MAC
- Clock counter
- FIFOs
- ...

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Slide 10
DSE (system level): Flexible integration of HWACCs

- L1-cache, external SDRAM
- Instruction set extensions
- Hardware accelerators
- Generic interface for external hardware extension
FPGA prototype based on RAPTOR system
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- 128 MSPS A/D converter
- Spartan-3 ADSP FPGA for data pre-processing
- Modular approach
- 0 - 5 GHz transceivers
ASIC prototype in 65nm

- Standard cell implementation
- 65 nm STMicroelectronics
- 400 MHz
- 2.7 mm² area requirements
- 32 kB L1-Cache
- ~100 mW power consumption
DSE (NoC level) GigaNoC based on CoreVA CPU
DSE (NoC level) GigaNoC based on CoreVA CPU

- 2D mesh-topology
- Wormhole routing
- Highly scalable
- Packet switching
- 5 I/O-ports per SB
- 750 MHz, 0.5 mm²/SB
- 24 Gbit/s link bandwidth
DSE (NoC level): IEEE 802.11b application

Scrambling
Diff. encoding
Symbol mapping

Fir-Filter
(I-Part)

Fir-Filter
(Q-Part)

Synchro-
nization

Packet Mem

Packet Mem

Packet Mem

Packet Mem

CoreVA

CoreVA

DSE (NoC level): IEEE 802.11b application

Clock cycles per Byte

Input data [Bytes]

CoreVA
CoreVA-NoC (1 PE)
CoreVA-NoC (2 PE)
CoreVA-NoC (4 PE)
Thank you for your attention

Dipl.-Ing. Thorsten Jungeblut

Cognitive Interaction Technology – Center of Excellence (CITEC), Bielefeld University
Universitätsstraße 21-23
33615 Bielefeld

Phone : +49 521 106-12103
Fax. : +49 521 106-12348
E-mail : tj@cit-ec.uni-bielefeld.de
www.cit-ec.de